Farzad Fatollahi-Fard

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SHORT BIOGRAPHY

Farzad Fatollahi-Fard is an FPGA Computing Systems Engineer in the Computer Architecture Group in the Computer Science Department at Lawrence Berkeley National Lab. He graduated from the University of California, Berkeley with a degree in Electrical Engineering and Computer Science. He spent several years designing FPGA platforms used in HPC applications for a startup company prior to coming the Lab. His research interests are focused on application co-design, custom HPC accelerators, and HPC on the edge.

EDUCATION

University of California, Berkeley **Berkeley, CA**
Bachelors of Science, Electrical Engineering and Computer Science *2009*

RESEARCH EXPERIENCE

Lawrence Berkeley National Lab
Computer Architecture Group (CAG) *2013–Present*

IARPA AGILE - Berkeley eXtensible Environment (BXE)

- Ported and analyzed program benchmarks on the RISC-V ISA using FireSim
- Added support for the RISC-V ISA to UPC++
- Deployed BXE infrastructure, a FPGA cloud-based computer architecture simulator using Chipyard and FireSim

Berkeley eXtensible Processing Engine (BXPE)

- FPGA-based edge network processing pipeline for real-time data processing using co-design
- In collaboration with ESnet, worked with NCEM and ALS to ingest data from scientific instruments at 100GbE link rate
- Implemented Center-of-Mass (NCEM) and Convolution (ALS) computation using the FPGA's DSP engines

OpenSoC Fabric

- On-chip network generation infrastructure
- Parameterizable and powerful on-chip network generator for evaluating future high performance computing architectures based on SoC technology
- Written in Chisel and modeled after existing state-of-the-art simulators

University of California, Berkeley
Research Accelerator for Multiple Processors (RAMP) *2008–2009*

- Design and began developing a fully IEEE754-Compliant Double Precision Floating Point Unit for Xilinx Virtex-5 FGPAs
- Design and develop firmware for the Xilinx SystemACE

EMPLOYMENT

Lawrence Berkeley National Lab **Berkeley, CA**
FPGA Computing Systems Engineer *2013–Present*

- Created the infrastructure for BXE, an on-premises cloud with FPGA-based hardware simulator
- Built and developed BXPE, a network-based co-designed processing engine
- Design, develop, maintain, and support OpenSoC Fabric, a parameterizable network-on-chip generator
- Design and assemble system-on-chip devices for high performance computing design space exploration
- Contribute and support tools developed for the CoDeX project
- Cross collaborate with sister labs in the Computer Architecture Lab

BEEcube, Inc. **Fremont, CA**

Hardware Engineer *2010–2013*

- Develop, maintain, and support embedded controller and firmware for BEE4 and miniBEE4 FPGA platform
- Design miniBEE4 platform, heading schematic capture and managed first prototype run
- Design daughter boards for BEE4 and miniBEE4, including multi-gigabit digital and analog boards

University of California, Berkeley, Berkeley Wireless Research Center (BWRC) **Berkeley, CA**

Junior Staff Engineer *2009–2010*

- Develop and maintain embedded controller for BEE3 FPGA platforms in which users can log in remotely, develop, and test designs
- Designed expansion board for embedded controller with USB FIFO, UART over USB, and PCIe for communication to FPGAs

SELECTED PUBLICATIONS

- **F. Fatollahi-Fard**, D. Donofrio, G. Michelogiannakis and J. Shalf, "OpenSoC Fabric: On-chip network generator," *2016 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Uppsala, 2016, pp. 194-203. doi: 10.1109/ISPASS.2016.7482094
- Khaled Z. Ibrahim, **Farzad Fatollahi-Fard**, David Donofrio, and John Shalf. 2016. Characterizing the Performance of Hybrid Memory Cube Using ApexMAP Application Probes. In *Proceedings of the Second International Symposium on Memory Systems* (MEMSYS '16). ACM, New York, NY, USA, 429-436. doi: 10.1145/2989081.2989090

LICENSES & CERTIFICATIONS

UC Berkeley Executive Education **Berkeley, CA**

Leading Complex Projects *April 2025*

Apply tools, frameworks, and strategies to manage traditional and complex projects. Evaluate and monitor performance in complex projects to achieve business objectives. Leverage adaptive leadership in complex projects to drive innovation. https://certificates.emeritus.org/9d3ff7d1-5e04-4530-8c0d-88b9e578dd7e

COMMUNITY SERVICE

- Steering Committee Member for Workshop on Open Source Supercomputing (OpenSuCo) at ISC17 and SC17 (2017)
- Organizing Committee Member for System-On-Chip for High Performance Computing Workshop (2014-2015)
- Tutorial on OpenSoC: A Flexible, Parameterizable, Open NoC Generation Tool at 8th International Symposium on Networks-on-Chip, NOCS2014 (2014)

AWARDS

Warren Y. Dere Design Award

http://www.eecs.berkeley.edu/Students/Awards/#dere *Spring 2010*

- Presented to a graduating senior in EECS whose accomplishment in engineering design is judged to be most outstanding

PROGRAMMING LANGUAGES & SKILLS

Knowledge in Chisel, Chipyard, FireSim, Scala, Verilog, VHDL, C, C++, Java, MATLAB, LabView, JavaScript, Perl, Python, and PHP

Skills in FPGAs, oscilloscopes, multimeters, spectrum analyzer, DC power supplies, soldering, crimping, CAD, Tensilica Processor Generator, OrCAD and Allegro PCB schematic capture and layout

Leadership skills in Understanding Complexities, Risk Management, Navigating Power, Adaptive Intelligence, and Social Intelligence